GI/ITG/GMA Technical Committee "Dependability and Fault Tolerance"

Call for Papers

16th Workshop on Dependability and Fault Tolerance (VERFE 2021)

in conjunction with **34th ARCS 2021,** virtual, June, 2021

Background and Focus Although the basic reliability of hardware and software components has improved over decades, their increasing number causes severe problems. Moreover, in recent years it can be observed that an increasing number of devices are integrated into environments of other physical components such as automotive or digital systems. Here, the complexity and number of interactions with these components creates problems with regard to maintaining a dependable operation of the entire system in case of faults or external disturbances. While this is not a problem with microprocessors, shrinking feature sizes, higher complexity, lower voltages, and higher clock frequencies increase the probability of design, manufacturing and operational faults, making fault tolerance techniques in general purpose processors to be of crucial importance in the future. As simple solutions (such as TMR) can easily get too expensive, the ability to trade increased reliability against performance/power overhead will become important, resulting in light-weight fault tolerance techniques implemented in hardware, but controllable from higher software layers.

This workshop aims at presenting contributions and work-in-progress from the research area of dependable and fault-tolerant computing in order to bring together scientists working in related fields.

Topics Contributions on the topic of "Dependable Embedded Systems" are of particular interest; contributions on general topics of dependability and fault tolerance are also welcome but not limited to:

- dependable computer systems, networks and embedded systems
- dependability of mechatronic systems
- fault-tolerant systems and system components
- safety-critical applications
- highly available systems
- real-time and performance guarantees
- testing of hardware and software
- fault detection and fault treatment
- failure prediction
- modeling, simulation and evaluation of fault-tolerant systems
- reliability models for hardware and software
- validation and verification
- fault models and fault abstraction
- fault injection techniques
- on-chip fault-tolerance
- software-controlled fault tolerance
- fault-tolerant processor architecture
- fault-tolerance in operating systems, storage and database systems

The workshop will focus on research presentations as well as brainstorming sessions.
Therefore, two kinds of contributions are welcome:

- research papers documenting results of scientific investigations and
- position papers proposing strategies or discussing open problems.

Informations for Authors
Accepted papers will be published by VDE and IEEExplore.
Papers should be in English and formatted according to IEEE eXpress "conference mode".
Selected papers will appear in the printed issue of the GI-FERS communications (ISSN **0724-5319)**.

Deadlines:

Submission:	**April 15th, 2021** (ext. abstracts (3-4 pages) or full papers (max. 8 pages), PDF) to: `bernhard.fechner@fernuni-hagen.de`
Notification:	**May 10th, 2021**
Camera-ready:	**May 24th, 2021** (max. 8 pages)

Workshop site: `https://arcs-conference.org/workshops`

Workshop Chairs

Bernhard Fechner	University of Hagen	Germany
Peter Sobe	HTW Dresden	Germany
Karl-Erwin Großpietsch	St. Augustin	Germany

Program Committee (TBC)

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